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| 09/648,540 | 08/28/2000 | Alexander D. Schapira | CA7010652001 | 7789 |

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| EXAMINER | |
|---|---|
| GUILL, RUSSELL L | |
| ART UNIT | PAPER NUMBER |
| 2123 | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/648,540 | SCHAPIRA ET AL. | |
| | Examiner | Art Unit | |
| | Russ Guill | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,2,3,4,8 and 13-18* is/are allowed.

6)☒ Claim(s) *5-7 and 9-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This Office Action is in response to an Amendment filed April 11, 2008. Claims 1 - 18 are pending. Claims 1 - 18 have been examined. Claim 5 - 7 and 9 - 12 are rejected. Claims 1 - 18 are allowable over the prior art of record.

2. If the Applicant feels that a telephone conversation would be useful, then the Applicant is invited to call the Examiner.

*Response to Remarks*

3. Regarding **claims 5 - 7 and 9 - 12** rejected under 35 USC § 112, first paragraph:

a. Applicant's arguments have been fully considered, but are not persuasive, as discussed below. Accordingly, the rejections are maintained.

b. The Applicant argues:

c. Claims 5-7 and 9-12 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Applicants respectfully traverse.

d. Applicants respectfully point to several examples in the Specification which provide clear written description to enable one of ordinary skill in the art to make and use the claimed invention. Applicants further respectfully note that the following examples are provided for illustration and explanation purposes only and do not intend to limit the scope of the claimed invention *as* embodied in these claims.

e. Applicants first respectfully point top. *3, I. 20-p. 4, I. 6* which provides, *as* some background information and to the extent pertinent, that "Mlle value 'Z', however, does not represent a state of either 0 or 1. The value 'Z' . represents the state of a signal not being driven or floating... When not actively driving a signal, an electronic device, such as a logic gate or other digital circuit, may present a high-impedance state, or 'Z' state, at its output. . . ."

f. Applicants then respectfully point to p. *13, 11. 10-16* which illustrate some embodiments of the claimed invention. These passages show that when an analog circuit block receives a Z value (i.e.,

floating value) of an input (i.e., the input is not being driven), simulator 100 enables the analog circuit block to **solve for that node** as if It **were an output** of the analog block. *P. 19, 1. 18-p. 20, 1.* 7 further illustrates that, in some embodiments, when input to analog block 203 is a Z value then such an input to analog circuit block 203 is not being driven by another device or circuit (). In this case, simulator 100 solves for the analog circuit block 203 absent the input to analog block 203 and propagates the analog block solution (i.e., signal value) to other fanouts of net 202 using the output **portion of the analog ioput.** These passages clearly provide sufficient written description to enable one of ordinary skill in the art to make and use the claimed invention *as* encompassed in claim 5 which, in part, recites "simulating the circuit design by modeling at least one of said output . . . as an **analog output signal** from said analog circuit to said node when said at least one of said output is in said high impedance state" (emphasis added.)

g. In addition, Applicants respectfully point to p. 12, 1. 16-p. 13, 1. 9 which states, to the extent pertinent, "when digital gate 201 drives any non-Z value onto network node 202, every fanout of net 202 including analog circuit block 203 connected to net 202 (analog block 203 in this example includes, among other things, components RI/R2 and transistor devices M1/M2) receive this non-Z value as an input. However, when digital gate 201 is not driving an output signal of 0, 1, or X, digital gate 201 presents a Z value (i.e., floating) output onto net 202 . . . ." That is, when the digital gate 201 drives any non-Z value (i.e., not floating or not in high impedence state), every fanout of net 202 including analog circuit block 203 receives this non-Z value as an input rather than output as illustrated in the preceding paragraph immediately above when the digital circuit block is not driving any non-Z values. Applicants therefore respectfully submit that these exemplary paragraphs clearly provide sufficient written description for the claimed invention of the independent claim 5 which recites, to the extent pertinent, "simulating the circuit design by modeling at least one of said output as a digital **output signal** from the corresponding digital circuit to said node when said at least one of said output is **not in said high impedance state** . .." (emphasis added.)

h. Therefore, Applicants respectfully submit that since claim 9 recites similar limitations as does claim 5, and claims 6-7 and 10-12 depend from claims 5 and 9 respectively, claim 5-7 and 9-12 are believed to have satisfied the requirements under 35 U.S.C. § 112, first paragraph. Applicants thus respectfully request the withdrawal of the rejections and reconsideration of these claims.

i. The Examiner respectfully replies:

ii. The Examiner appreciates the Applicant's argument, but respectfully disagrees as follows. The arguments do not appear to approach the issue in the rejection. The claim appears to set the output to an analog value when only one of the digital outputs is high impedance, but the specification appears to require that all of the digital outputs must be high impedance in order to set the output to an analog value.

4. Regarding **claims 3 - 4** rejected under 35 USC § 112, second paragraph:

a. Applicant's arguments have been fully considered, and are persuasive, as discussed below. Accordingly, the rejections are withdrawn.

b. The Applicant argues:

c. Claim 3 recites, to the extent pertinent, "simulating the circuit design by modeling said output as a **digital output signal from said** digital circuit to said node when said output is not in **said high impedance** state, and as an **analog output signal from** said analog circuit to said node **when said output is in said high impedance state"** (emphasis added.) That is, the above limitation explicitly states that when the output is in a high impedance state, the method models the output as an analog output signal from the analog circuit to the node, and that when the output is not in the high impedance state, the method models the output as a digital output signal from the digital circuit to the node. That is, depending upon whether the output is in a impedance state, the method models the output as an analog output signal from the analog circuit or *as a* digital output signal from the digital circuit.

d. As such, claim 3 does not assign both a high impedance state value and an analog signal value to the output as alleged by the Office Action. Applicants thus respectfully request withdrawal of the rejections and reconsideration of these claims.

i. The Examiner respectfully replies:

ii. After further discussion with senior examination staff, the arguments are persuasive

5. Regarding claim 17 rejected under 35 USC § 112, second paragraph:

a. Applicant's arguments have been fully considered, and are persuasive. Accordingly, the rejection is withdrawn.

*Claim Rejections - 35 USC § 112*

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

a. **Claims 5 - 7 and 9 - 12** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. One reasonably skilled in the art could not make or use the invention from the disclosure in the specification, coupled with information known in the art, without undue experimentation, for the following reasons:

i. Regarding independent claim 5 and dependent claims, claim 5 recites in the second limitation, "simulating the circuit design by modeling at least one of said output as a digital output signal from the corresponding digital circuit to said node when said at least one of said output is not in said high impedance state, and as an analog output signal from said analog circuit to said node when said at least one of said output is in said high impedance state". The specification appears to teach that

all of the outputs of the plurality of digital circuits must be in a high impedance state in order for the analog output signal to be the final output (*refer to figure 4, and page 21, lines 11 – 22 through page 22, lines 1 – 11*). Further, the specification appears to teach that the plurality of outputs is resolved to a single value by the simulation, and that the single value is used to determine whether the final output is analog or digital. Further, the specification appears to teach that when the final output is analog, that a digital state value is also provided to any digital circuits using the output. Claim 6 also appears to recite that only "at least one of said output is in said high-impedance state" is needed for an analog output signal. Claim 7 appears to collectively resolve the digital circuit outputs into a single output signal, but does not appear to use the signal to determine whether an analog signal is output.

ii. Regarding independent claim 9 and dependent claims, claim 9 recites in the second limitation, "simulating the circuit by modeling at least one of said output provided by said one or more digital circuits as a digital output signal from the corresponding digital circuit to said node when said at least one of said output is not in said high impedance state, and as an analog output signal from said analog circuit to said node when said at least one of said output is in said high impedance state". The specification appears to teach that all of the outputs of the plurality of digital circuits must be in a high impedance state in order for the analog output signal to be the final output (*refer to figure 4, and page 21, lines 11 – 22 through page 22, lines 1 – 11*). Further, the specification appears to teach that the plurality of outputs is resolved to a single value by the simulation, and that the single value is used to determine whether the final output is

analog or digital. Further, the specification appears to teach that when the final output is analog, that a digital state value is also provided to any digital circuits using the output. Claims 10 - 11 also appear to recite that only "at least one of said output is in said high-impedance state" is needed for an analog output signal. Claim 12 appears to collectively resolve the digital circuit outputs into a single output signal, but does not appear to use the signal to determine whether an analog signal is output.

*Allowable Subject Matter*

7. Claims 1 – 18 are allowable over the prior art of record.

8. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

9. A reasons for indicating allowability of the claims was provided in previous Office Actions dated August 21, 2006 and March 21, 2006.

*Conclusion*

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

11. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date

of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russ Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday – Friday 9:30 AM – 6:00 PM.
13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.
14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG

/Paul L Rodriguez/
Supervisory Patent Examiner,
Art Unit 2123